AMENDMENTS

This section presents changes to the specification in a clean-unmarked format. A version with markings to show the changes made by the current amendment is provided after the remarks section. (In the present Response there are no amendments to the specification.)

In The Claims:

No claims are amended, cancelled, or added by this amendment.

Presentation Of The Claims In A Clean-Unmarked Format

17. A method of forming an interconnect structure, comprising:

forming a first layer of a first dielectric material on a substrate;

patterning the first layer;

depositing conductive material over the patterned first layer;

planarizing the conductive material such that a plurality of interconnect lines are formed including a first and a second power interconnect lines and a third and fourth signal interconnect lines;

forming a mask layer over the interconnect lines and patterned first layer;

patterning the mask layer such that the first and second power interconnect lines and a first portion of the patterned first layer are covered, and the third and fourth signal interconnect lines and a second portion of the patterned first layer are uncovered;

removing the dielectric material from the uncovered portion;

removing the second portion of the patterned first layer; and

depositing a second layer of a second dielectric material between the third and fourth signal interconnect lines, the second dielectric material having a smaller dielectric constant than the first dielectric material.

20. A method of forming an interconnect structure, comprising:

forming a first layer of a conductive material on a substrate;

forming a first pair of power interconnect lines to distribute power and a second pair of signal interconnect lines to carry signals from the conductive material;

depositing a first dielectric material over and between the first pair and the second pair;

forming a mask layer over the first pair and the second pair and first dielectric material;

patterning the mask layer such that one portion of the dielectric material between one pair is covered and another portion of the dielectric material between another pair is uncovered;

removing the portion of the dielectric material that is uncovered;

removing the patterned mask layer; and

depositing a second dielectric material having a different dielectric constant than a dielectric constant of the first dielectric material.

21. The method of Claim 20, wherein the first dielectric material has a dielectric constant greater than a dielectric constant of the second dielectric material.

22. The method of Claim 20, wherein the first dielectric material has a dielectric constant less than a dielectric constant of the second dielectric material.

23. A method of making in-plane decoupling capacitors, comprising:

forming a first plurality of conductive power lines on an insulating substrate, the first plurality of conductive power lines having a first dielectric therebetween; and

forming a second plurality of conductive signal lines on the insulating substrate, the second plurality of conductive signal lines having a second dielectric therebetween;

wherein the first dielectric has a dielectric constant greater than a dielectric constant of the second dielectric.

24. A method of forming an interconnect structure, comprising:

forming, on a substrate, a first plurality of signal interconnect lines and a first intralayer dielectric disposed between the first plurality of signal interconnect lines;

removing a portion of the first intralayer dielectric;

forming a second intralayer dielectric on the substrate where the first intralayer dielectric was removed; and

forming a second plurality of power interconnect lines in the second intralayer dielectric.

25. The method of Claim 24, wherein a dielectric constant of the first intralayer dielectric is different from a dielectric constant of the second intralayer dielectric.

26. The method of Claim 25, wherein forming the second plurality of power interconnect lines comprises etching trenches in the second intralayer dielectric, depositing a conductive material, and polishing the conductive material such that the conductive material is substantially removed except for that which is in the trenches.

27. A method of forming an interconnect structure, comprising:

forming a first dielectric layer on a substrate;

removing a portion of the first dielectric layer;

forming a second dielectric layer on the substrate where the portion of the first dielectric layer was removed; and

forming a plurality of signal lines in the first dielectric layer and a power line in the second dielectric layer.

28. The method of Claim 27, wherein a dielectric constant of the first dielectric is different from a dielectric constant of the second dielectric.

29. The method of Claim 28, wherein forming the plurality of signal lines and the power line comprises etching trenches in the first and the second dielectrics, depositing a conductive material, and polishing the conductive material such that the conductive material is substantially removed except for that which is in the trenches.

30. An integrated circuit device comprising a substrate having an interconnect structure formed thereon by the method of Claim 17.

31. The method of Claim 20, wherein the one pair that is covered comprises the first pair of power interconnect lines and wherein the second dielectric material has a lower dielectric constant than the first dielectric material.

32. The method of Claim 20, wherein the one pair that is covered comprises the second pair of signal interconnect lines and wherein the second dielectric material has a higher dielectric constant than the first dielectric material.

33. A semiconductor device comprising a substrate having an interconnect structure formed thereon by the method of Claim 20.

34. An integrated circuit device comprising an insulting substrate having formed thereon in-plane decoupling capacitors made by the method of Claim 23.

35. The method of Claim 24, wherein the second intralayer dielectric has a larger dielectric constant than the first intralayer dielectric.

36. A integrated circuit device comprising a substrate having an interconnect structure formed thereon by the method of Claim 24.

37. A integrated circuit device substrate comprising an interconnect structure formed thereon by the method of Claim 27.

38. A method comprising:

providing an integrated circuit substrate; and

making on the integrated circuit substrate an interconnect structure comprising a first pair of interconnect lines to distribute power having a first material disposed therebetween and a second pair of interconnect lines to carry signals having a second material disposed therebetween, wherein the first dielectric material has a first dielectric constant that is greater than a second dielectric constant of the second material.

39. The method of Claim 38, wherein making includes making the interconnect structure comprising the first pair of interconnect lines that are separated by a first distance and the second pair of interconnect lines that are separated by a second distance that is substantially the same as the first distance.

40. The method of Claim 38, wherein making includes removing a portion of second material deposited between the first pair of interconnect lines and depositing the first material where the second material was removed.

41. The method of Claim 40, wherein making comprises protecting a second portion of the second material between the second pair of interconnect lines with a mask.

42. The method of Claim 38, wherein making includes removing a portion of first material deposited between the second pair of interconnect lines and depositing the second material where the first material was removed.

43. The method of Claim 42, wherein making comprises protecting a second portion of the second material between the second pair of interconnect lines with a mask.

44. An integrated circuit comprising an interconnect structure made by the method of Claim 38.